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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/489,895	01/24/2000	Jorg Henkel	A7544	6422

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	7

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/489,895	Applicant(s) HENKEL ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-8 have been presented for examination. Claims 1-8 have been examined and rejected.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The abstract of the disclosure is objected to because the number of words exceeds 150.

Correction is required. See MPEP § 608.01(b), and ...

6.02 Content of Specification
(j) Abstract of the Disclosure: A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:
Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. **Claims 6-8** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 6-8 recite a computer program product. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

Function A

Function B

Function C, etc...

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Independent **Claims 1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kageshima U.S. Patent 6,096,089** in view of **Catthoor et al. U.S. Patent 6,223,274.**

4.1 As regards independent **Claims 1 and 2** the *Kageshima* reference discloses a method of power estimation of a core-model **(Figure 1),** capturing gate-level simulation data **(Figure 2),** deploying the captured gate-level simulation data where this data correlates to a plurality of instructions to obtain power estimations for each instruction **(Figure 11).**

However, the *Kageshima* reference does not expressly disclose an embedded system or system-on-a-chip.

The *Catthoor et al.* reference discloses a method of calculating the energy consumption of an embedded system or system-on-a-chip **(Figures 4, 6, 16, 20, Col. 3 Lines 49-53, Col. 5 Lines 54-59).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Catthoor et al.* reference because of the problems in industry related to the development of fast video chips that are also power efficient. Large ASICs with on-board embedded processors consume a great deal of energy and it is important for portable device, such as laptops, to be energy efficient so that they will not exhaust their limited supply of battery power **(*Catthoor et al.*, Col. 2 Lines 1-16).**

5. Dependent **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kageshima U.S. Patent 6,096,089** in view of **Catthoor et al. U.S. Patent 6,223,274** and in further view of **Dean et al. U.S. Patent 6,397,170.**

5.1 As regards independent **Claim 2** see paragraph **4.1** above.

5.2 As regards dependent **Claim 3** the *Kageshima* reference does not expressly disclose toggle counts in a power estimation simulator.

The *Dean et al.* reference discloses toggle counts in a power estimation simulator **(Figure 1).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Dean et al.* reference

because by including the toggle counts in the power estimation the power calculation be come more accurate **(Dean et al. Col. 2 Lines 7-20).**

6. Independent **Claim 4** and dependent **Claim 5** are being rejected under 35 U.S.C. 103(a) as being unpatentable over **Kageshima U.S. Patent 6,096,089** in view of **Catthoor et al. U.S. Patent 6,223,274** and in further view of **Dean et al. U.S. Patent 6,397,170.**

6.1 As regards independent **Claim 5** the *Kageshima* reference discloses a method of power estimation of a core-model **(Figure 1),** capturing gate-level simulation data **(Figure 2),** deploying the captured gate-level simulation data where this data correlates to a plurality of instructions to obtain power estimations for each instruction **(Figure 11).**

However, the *Kageshima* reference does not expressly disclose an embedded system or system-on-a-chip.

The *Catthoor et al.* reference discloses a method of calculating the energy consumption of an embedded system or system-on-a-chip **(Figures 4, 6, 16, 20, Col. 3 Lines 49-53, Col. 5 Lines 54-59).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Catthoor et al.* reference because of the problems in industry related to the development of fast video chips that are also power efficient. Large ASICs with on-board embedded processors consume a great deal of energy and it is important for portable device, such as laptops, to be energy efficient so that they will not exhaust their limited supply of battery power **(*Catthoor et al.*, Col. 2 Lines 1-16).**

6.2 As regards dependent **Claim 5** the *Kageshima* reference does not expressly disclose using a hardware description language.

The *Dean et al.* reference discloses a hardware description language **(Col. 2 Lines 21-37).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Kageshima* reference with the *Dean et al.* reference because, HDL's are used to model modern VHLIC circuit designs and therefore an artisan in the circuit design area is required to know how to design using these design tools **(Dean et al. Col. 2 Lines 65-67, Col. 3 Lines 1-10).**

7. Independent **Claims 6, 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Loucks et al. U.S. Patent 5,828,576** in view of **Catthoor et al. U.S. Patent 6,223,274.**

7.1 As regards independent **Claims 6, 7 and 8** the *Loucks et al.* reference discloses an object oriented method of modeling a circuit design for the purpose of monitoring power consumption **(Figures 5A-5L, 10, 10A, 10B, 10C, 11, Col. 3 Lines 60-67, Col. 4 Lines 1-35).**

However, the *Loucks et al.* reference does not expressly disclose simulating an embedded system or system-on-a-chip.

The *Catthoor et al.* reference discloses a method of calculating the energy consumption of an embedded system or system-on-a-chip **(Figures 4, 6, 16, 20, Col. 3 Lines 49-53, Col. 5 Lines 54-59).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Loucks et al.* reference with the *Catthoor et al.* reference

because of the problems in industry related to the development of fast video chips that are also power efficient. Large ASICs with on-board embedded processors consume a great deal of energy and it is important for portable device, such as laptops, to be energy efficient so that they will not exhaust their limited supply of battery power **(*Catthoor et al.*, Col. 2 Lines 1-16).**

Conclusion

8. **Claims 1-8** have been examined and rejected. This action is **NON-FINAL.**

8.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER